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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/643,380	08/21/2000	Manoj Khare	42390.P9301	8768

7590   09/26/2003

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EXAMINER
TRAN, DENISE

ART UNIT	PAPER NUMBER
2186	9

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1.   The applicant's amendment filed 7/11/03 has been considered. Claims 1-26 are

pending in this Office Action.

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Sharma et al., U.S. Patent No. 6,085,263, hereinafter Sharma in view of Lewchuk et al.,

U.S. Patent No. 6,058,461, hereinafter Lewchuk.

As per claim 1, Sharma teaches the use of an apparatus comprising:

a prefetch engine to prefetch data from a distributed, coherent memory in

response to a first transaction from an input/output bus directed to the distributed,

coherent memory (e.g. abstract and col. 13, lines 20-42); and

an input/output coherent cache buffer to receive the prefetched data, the

coherent cache buffer being coherent with the distributed, coherent memory and with

other cache memories in a system including the input/output coherent cache buffer (e.g.

abstract and col. 13, lines 20-42),

the prefetch engine further to prefetch data for the memory transactions from the

I/O bus (abstract; figure 8, elements 810, 140). Sharma does not specifically show the

use of speculatively prefetch data if data has been prefetched for pending, memory-related transactions. Lewchuk shows the use of speculatively prefetching data if data has been prefetched for pending, memory-related transactions (i.e., prefetched transactions have a higher priority than speculatively prefetched transactions, therefore speculatively prefetched transactions can only occur if there are no pending prefetched transactions in an input request queue) (e.g. abstract, lines 4-10 and col. 2, lines 9-15; col. 8, lines 55-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Lewchuk with Sharma because it would provide for a reduction in memory access time by speculating subsequent hits in the cache and provide for a reduction in latency for performing normal memory operations before speculative operations and improve performance of the computer system, as taught by Lewchuk col. 2, lines 65-67.

As per claim 2, Sharma teaches the use of the prefetch operation performed by the prefetch engine is a non-binding prefetch operation such that the prefetched data received by the coherent cache buffer may be altered by a memory in the distributed coherent memory (e.g. col. 7, lines 20-23 and figure 9).

As per claim 3, Sharma teaches the use of the first transaction request is a memory read request and the prefetch engine issues a read request to prefetch data to be read from the distributed, coherent memory in response to the first transaction request (e.g. col. 5, lines 7-47).

As per claim 4, Sharma teaches the use of the first transaction request is a memory write request and the prefetch engine issues a request to prefetch ownership of a memory line in the distributed, coherent memory, the memory line being indicated by the first transaction request (e.g. col. 5, lines 18-21 and col. 7, lines 24-38).

As per claim 5, Sharma teaches the use of an input/output transaction request buffer to temporarily store transaction requests received from the input/output bus directed to the distributed, coherent memory (e.g. figure 2, elements 212 to 228 and figure 10, elements 812, 814).

As per claim 6, Sharma teaches the use of the prefetch engine prefetches data in response to transaction requests stored in the input/output transaction request buffer (e.g. abstract and col. 14, lines 9-37).

As per claim 7, Sharma teaches the use of the prefetch engine prefetches data in response to transaction requests stored in the input/output transaction request buffer regardless of the order in which the transaction requests were received from the input/output bus (e.g. abstract and col. 14, lines 9-37).

As per claim 8, Sharma teaches the use of a retire engine to retire input/output transaction requests stored in the transaction request buffer in program order after the transaction requests have been completed (e.g. abstract and col. 14, lines 9-37).

As per claim 9, Sharma teaches the use of the retire engine is further to check the input/output coherent cache buffer to determine whether data associated with an input/output transaction request to be retired is present in the input/output coherent cache buffer in a valid state (e.g. col. 14, line 61 to col. 15, line 6).

As per claim 10, Sharma teaches the use of coherency is maintained between the input/output coherent cache buffer and the distributed, coherent memory using a MESI protocol (e.g. col. 7, lines 24-40 and col. 8, lines 8-30).

As per claim 11, Sharma teaches a method comprising:

prefetching data in response to a first input/output transaction request received from an input/output bus and directed to a distributed, coherent memory (e.g. abstract and col. 13, lines 20-42);

prefetched data for pending memory –related input/output transactions (e.g., abstract);

temporarily storing the prefetched data(e.g. abstract and col. 13, lines 20-42); and

maintaining coherency between the prefetched data and data stored in the

distributed, coherent memory and data stored in other cache memories (e.g. abstract

and col. 13, lines 20-42; fig. 1, caches122-124; col. 7, lines 24-40 and col. 8, lines 8-30).

Sharma does not specifically show the use of if data has been prefetched for pending

memory transactions, speculatively prefetching data. Lewchuk shows the use of if data

has been prefetched for pending memory transactions, speculatively prefetching data

(i.e., prefetched transactions have a higher priority than speculatively prefetched

transactions, therefore speculatively prefetched transactions can only occur if there are

no pending prefetched transactions in an input request queue) (e.g. abstract, lines 4-10

and col. 2, lines 9-15; col. 8, lines 55-68). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to combine Lewchuk with Sharma

because it would provide for a reduction in memory access time by speculating

subsequent hits in the cache and provide for a reduction in latency for performing

normal memory operations before speculative operations and improve performance of

the computer system, as taught by Lewchuk col. 2, lines 65-67.

As per claim 12, Sharma teaches buffering input/output transaction requests

received from the input/output bus that are directed to the distributed, coherent memory

(e.g., col. 8, lines 40-55 and col. 14, lines 10-37).

As per claim 13, Sharma teaches the use of prefetching data in response to second and third buffered input/output transactions wherein prefetching data in response to the first, second and third buffered input/output transactions may be performed in any order (e.g. abstract and col. 14, lines 9-60).

As per claims 14-15, Sharma teaches the use of retiring the buffered input/output transactions in the order in which they were issued by the input/output bus (e.g. abstract and col. 14, lines 9-37); the use of the checking the temporarily stored, prefetched data to determine whether valid data corresponding to the transaction request to be retired is temporarily stored (e.g. col. 14, line 61 to col. 15, line 6).

As per claims 16-18, Sharma teaches maintaining coherency using a MESI protocol (e.g. col. 7, lines 24-40 and col. 8, lines 8-30); prefetching including: issuing a request for the data in response to the first transaction request, and receiving the requested data (e.g. col. 5, lines 7-47); and prefetching data in response to a second input/output transaction request received from the i/o bus and directed to the distributed, coherent memory occurs between issuing the request and receiving the requested data (e.g. col. 5, lines 18-21 and col. 7, lines 24-38).

As per claim 19, it is rejected for similar reasons as stated above. Furthermore, Sharma teaches the use of a computer system comprising:

first and second processing nodes each including at least one processor and at

least one caching agent (e.g. figure 1, elements 102-106);

a distributed coherent memory wherein portions of the distributed coherent

memory are included within each of the first and second processing nodes (e.g. figure

1, elements 122-128 and col. 13, lines 30-40); and

an input/output node coupled to the first and second processing nodes (e.g.

figure 1, element 800), the input/output node comprising:

a prefetch engine to prefetch data from a distributed, coherent memory in

response to a first transaction from a first input/output bus directed to the distributed,

coherent memory (e.g. abstract and col. 13, lines 20-42) and to prefetch data for

pending memory-related transactions from the input/output bus (e.g., abstract and fig. 8,

els. 810, 812, 872, 140); and

an input/output coherent cache buffer to receive the prefetched data, the

coherent cache buffer being coherent with the distributed, coherent memory and the

caching agents (e.g. abstract and col. 13, lines 20-42). Sharma does not specifically

show the use of speculatively prefetch data after data has been prefetched for pending

memory-related transactions. Lewchuk shows the use of speculatively prefetching data

after data has been prefetched for pending memory-related transactions (i.e.,

prefetched transactions have a higher priority than speculatively prefetched

transactions, therefore speculatively prefetched transactions can only occur if there are

no pending prefetched transactions in an input request queue) (e.g. abstract, lines 4-10

and col. 2, lines 9-15, col. 8, lines 55 to 68). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to combine Lewchuk with

Sharma because it would provide for a reduction in memory access time by speculating

subsequent hits in the cache and provide for a reduction in latency for performing

normal memory operations before speculative operations and improve performance of

the computer system, as taught by Lewchuk col. 2, lines 65-67.

As per claim 20, Sharma teaches the use of a coherent system interconnect to

couple each of the first and second processing nodes to the input/output node, the

coherent system interconnect to communicate information to maintain coherency of the

distributed, coherent memory and to maintain coherency between the input/output

coherent cache buffer and the distributed, coherent memory (e.g. figure 1 and col. 7,

line 10 to col. 8, line 40).

As per claim 21, Sharma teaches coherency is maintained using a MESI protocol

(e.g. col. 7, lines 24-40 and col. 8, lines 8-30

As per claim 22, Sharma teaches the use of an interconnection network to

communicate information between the first and second processing nodes and the

input/output node (e.g. figures 1 and 4).

As per claim 23, Sharma teaches the use of an input/output bridge coupled between the first and second processing nodes and a plurality of input/output buses, the plurality of input/output buses including the first input/output bus, the input/output bridge including the prefetch engine and the input/output coherent cache buffer (e.g. figure 1, elements 102, 800 and 130, and figure 4).

As per claims 24, Sharma teaches the use of the input/output bridge comprising at least one i/o transaction requests received from the plurality of i/o buses that are directed to the distributed, coherent memory (e.g. figure 1, elements 102, 800 and 130, and figure 4; figure 2, elements 212 to 228 and figure 10, elements 812, 814).

As per claim 25, Sharma teaches the use of the prefetch engine prefetches data in response to transaction requests stored in the input/output transaction request buffer regardless of the order in which the transaction requests are stored (e.g. abstract and col. 14, lines 9-37).

As per claim 26, Sharma teaches wherein the i/o bridge further comprising: a retire engine to check the input/output coherent cache buffer for valid data corresponding to a transaction request to be retired (e.g. col. 14, line 61 to col. 15, line 6) and the retire engine to retire transaction requests stored in the i/o transaction request buffer in program order (e.g. abstract and col. 14, lines 9-37).

4.   Applicant's remarks filed 7/11/03 have been considered, but are moot in view of

the new grounds of rejection.

5.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

6.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

a)   Buckland et al. (6581129) is cited to show speculative pre-fetching.

7.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Denise Tran whose telephone number is (703) 305-

9823. The examiner can normally be reached on Monday, Thursday and an alternated

Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 872-9306 for

central Official communications and (703) 746-7240 for Non Official communications.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 305-

3900.

D.T.
September 21, 2003